

Re: about clock register setting

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 - *Date:* Wed, 23 Jan 2008 09:33:40 -0500
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Explaining line by line would take pages of information. Could you narrow it down by telling us what you don't understand?

I will give you a quick overview of what is going on.

1. You have a structure which maps to how the registers are layed out in the hardware
2. You have a pointer to the structure
2. The pointer to the stucuture is mapped to the base address of some part of the hardware
3. By dereferencing the pointer to the strucutre, you are reading/writing the register in hardware
4. The registers are defined in the PXA270 Developer's Manual where you can get all of the detail for the hardware.

—
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"daniel" <daniel@xxxxxxxxxxxxxxxxxxxxxxxxxxxx> wrote in message
news:4ADB7896-5EDB-4F8A-9B36-88359C02FB4E@xxxxxxxxxxxxxxxxxxxx

I'm not familiar with hardware register control.
During reading my pxa 27x BSP, I got reached a very hardware specific code about system clock manager setting like following.

```
// pCLKRegs is a Clock manager's address and cccr is Core Clock  
Configuration register  
if ((pCLKRegs->cccr & 0x1F) < 16)  
{  
    // If do not change to 91Mhz, do not need to change mdfref.  
    //pMEMC->mdrefr &= ~(0xFFF);
```

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```
//pMEMC->mdrefr =  
((0x1<<29)|(0x1<<20)|(0x1<<17)|(0x1<<16)|(0x1<<13)|0x31);  
pMEMC->mdcnfg = 0xA000AC9;  
pMEMC->mdrefr = 0x2013A031;  
pMEMC->msc0 = 0x15D095D2;  
}
```

Is there any kind teacher who will let me know the code line by line? Or introduce any material which I should first study.
Thank you in advance.