

## Re: PXA270 I2C register mapping

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*Source:*

<http://www.tech-archive.net/Archive/WindowsCE/microsoft.public.windowsce.embedded/2008-05/msg00243.html>

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- *From:* shai <shaihi@xxxxxxxx>
  - *Date:* Mon, 26 May 2008 22:36:20 -0700 (PDT)
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Anyone knows?

Thanks

On May 25, 4:49 pm, shai <sha...@xxxxxxxx> wrote:

Hi,

I wanted to ask if someone can explain to me how the following mapping works without a problem:

In the spec, the I2C registers are specified as:  
0x4030\_1680 IBMR I2C Bus Monitor register 9-30  
0x4030\_1684 reserved  
0x4030\_1688 IDBR I2C Data Buffer register 9-29  
0x4030\_168C reserved  
0x4030\_1690 ICR I2C Control register 9-23  
0x4030\_1694 reserved  
0x4030\_1698 ISR I2C Status register 9-26  
0x4030\_169C reserved  
0x4030\_16A0 ISAR I2C Slave Address register 9-28

When wanting to map them, the following code is used:

```
RegPA.QuadPart = BULVERDE_BASE_REG_PA_I2C;  
pI2CRegs =(volatile XLLP_I2C_T *) MmMapIoSpace(RegPA,  
sizeof(XLLP_I2C_T),FALSE);
```

when BULVERDE\_BASE\_REG\_PA\_I2C is 0x40300000.

the struct XLLP\_I2C\_T is defined as:

```
typedef struct
```

```
{  
    XLLP_VUINT32_T IBMR;          /* Bus monitor  
register */  
    XLLP_UINT32_T RESERVED1;     /* addr. offset 0x84-0x88 */  
    XLLP_VUINT32_T IDBR;        /* Data buffer Register */  
    XLLP_UINT32_T RESERVED2;     /* addr. offset 0x8C-0x90*/  
    XLLP_VUINT32_T ICR;         /* Global Control Register */  
    XLLP_UINT32_T RESERVED3;     /* addr. offset 0x94-0x98 */
```

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```
XLLP_VUINT32_T ISR; /* Status Register*/  
    XLLP_UINT32_T RESERVED4; /* addr. offset 0x9C-0xA0 */  
XLLP_VUINT32_T ISAR; /* Slave address register */
```

```
} XLLP_I2C_T, *P_XLLP_I2C_T;
```

And everything works fine and nice.

My question is ->

Where in the code I posted does the system take into account the 0x1680 offset between BULVERDE\_BASE\_REG\_PA\_I2C and the actual starting address of the I2C registers?

Thanks in advance,  
Shai